CLAIMS

1. A method of writing individual bits of data to a register, said method comprising:

receiving bits of data in a data field, the number of bits in the data field being equal to the number of bits in the register and bit locations in the data field corresponding respectively to bit locations in the register;

receiving enable bits in a bit enable field, the number of enable bits in the bit enable field being equal to the number of bits in the register and bit locations in the bit enable field corresponding respectively to bit locations in the register; and

overwiting only the bits at the bit locations of the register for which the enable bit in the corresponding location in the bit enable field is set with the bit in the corresponding location in the data field.

2. The method recited in claim 1, wherein the register is a control register for a data transfer operation.

3. The method recited in claim 2, wherein the data transfer operation transfers data to or from an IDE storage device.

4. The method recited in claim 3, wherein the control register is an IDE DMA status register.

5. The method recited in claim 3, wherein the control register is a command register.

6. The method recited in claim 1, wherein some of the bits of said register are not overwritten.

7. The method recited in claim 1, wherein the data field and the bit enable field are received simultaneously.

8. The method recited in claim 7, wherein the data field is provided at an address which is contiguous with the address for the bit enable field.

9. The method recited in claim 1, wherein the data transfer operation comprises an IDE data transfer between a processor subsystem and an external IDE storage device or peripheral.

10. The method recited in claim 9, wherein the processor subsystem posts

an entire command sequence for setting up the IDE data transfer.

11. The method recited in claim 9, wherein the method is carried out in an IDE controller in a bridge connected between the processor subsystem and the external IDE storage device or peripheral.

12. A computer comprising:

a processor subsystem;

a device which transfers data to or from said processor subsystem; and

a controller connected between said device and said processor subsystem and adapted to control the transfer of data between said device and said processor subsystem, said controller executing a method comprising,

receiving bits of data in a data field, the number of bits in the data field being equal to the number of bits in a control register in the controller and bit locations in the data field corresponding respectively to bit locations in the control register;

receiving enable bits in a bit enable field, the number of enable bits in the bit enable field being equal to the number of bits in the control register and bit locations in the bit enable field corresponding respectively to

bit locations in the control register; and

overwiting only the bits at the bit locations of the control register for which the enable bit in the corresponding location in the bit enable field is set with the bit in the corresponding location in the data field.

13. The computer recited in claim 12, further comprising a bridge between the processor subsystem and at least said device, the controller being included in the bridge.

14. The computer recited in claim 13, wherein the device comprises an IDE storage device and the bridge comprises an I/O controller hub (ICH) which controls an IDE data transfer between the processor subsystem and the IDE storage device.

15. The computer recited in claim 12, wherein the processor subsystem posts an entire command sequence in the controller for setting up the IDE data transfer.

16. A software program stored in a tangible medium, said program, when executed, causing a computer to execute a method of writing individual bits of data to a register, said method comprising:

receiving bits of data in a data field, the number of bits in the data field being equal to the number of bits in the register and bit locations in the data field corresponding respectively to bit locations in the register;

receiving enable bits in a bit enable field, the number of enable bits in the bit enable field being equal to the number of bits in the register and bit locations in the bit enable field corresponding respectively to bit locations in the register; and

overwiting only the bits at the bit locations of the register for which the enable bit in the corresponding locations in the bit enable field is set with the bits in the corresponding location in the data field.

17. The software program recited in claim 16, wherein said software program comprises a driver in the operating system software executed by a processor subsystem in the computer.

18. The software program recited in claim 17, wherein the register is a control register in a controller adapted to control an IDE data transfer operation between said processor subsystem and an IDE storage device.

19. The software program recited in claim 17, wherein the processor subsystem posts an entire command sequence for setting up the IDE data transfer to the controller.